What Is Claimed Is:

1. A method for transcribing at least one data record of an external data source to a processor unit; the at least one data record being transmitted from the external data source together with additional information to a buffer memory of the processor unit; a check of the admissibility of using the at least one data record being performed on the basis of the additional information; a blocking signal being generated when the check results in that the use is not allowed and then the at least one data record being deleted from the buffer memory; and an enable signal being generated when use of the at least one data record is allowed,
wherein the additional information (13) includes an identifier (15a, 15b, 15c, 15d) assigned individually to the processor unit (20), the check of the validity being performed in the processor unit (20).

2. The method as recited in Claim 1,
wherein an identifier (15a, 15b, 15c, 15d) is valid only once for checking an at least one transmitted data record (12) stored in the buffer memory (22).

3. The method as recited in one of Claims 1 or 2,
wherein when the enable signal has been generated, the at least one data record (12) is transmitted from the buffer memory (22) to a functional memory (26) from which it may be read for processing purposes.

4. The method as recited in Claim 3,
wherein the identifier (15a, 15b, 15c, 15d) together with the at least one data record (12) is stored in the functional memory (26) and the particular identifier (15a, 15b, 15c, 15d) is checked when calling up a data record (12) from the functional memory (26).

5. The method as recited in one of the preceding claims,
wherein a list of code words (25a, 25b, 25c, 25d) is stored in a code word memory (25) of the processor unit (20), the identifier (15a, 15b, 15c, 15d) being compared with the code word (25a, 25b, 25c, 25d) and validity being deduced when the code word (25a, 25b, 25c, 25d) and the identifier (15a, 15b, 15c, 15d) match, are identical in particular.

6. The method as recited in Claim 5,

wherein a counter content of a counter (24) is stored, the counter (24) pointing to a code word (25a, 25b, 25c, 25d) of the code word memory (25), and the counter content of the counter (24) being incremented before each check of the identifier (15a, 15b, 15c, 15d) of at least one data record (12) stored in the buffer memory (22).

7. The method as recited in one of the preceding claims,
wherein the processor unit (20) is identifiable by an identification sequence (14), the identification sequence (14) preferably also being part of the additional information (13) and being used in the validity check of the at least one data record (12).

8. The method as recited in one of the preceding claims,
wherein valid identifiers (15a, 15b, 15c, 15d) for the processor unit are stored in an identifier server (18).

9. The method as recited in one of the preceding claims,
wherein identifiers (15a, 15b, 15c, 15d) are retrievably stored in the code word server (18) for a plurality of counter contents of the counter (24), the identifiers (15a, 15b, 15c, 15d) being allocatable to a certain processor unit (20), in particular via an identification sequence (14).

10. A processor unit (20) having a buffer memory (22), a rewritable functional memory (26) which is accessed during the operation of the processor unit, both being designed for storing at least one data record (12), and having an interface (21) for importing of at least one data record (12) together with additional information (13) into the buffer memory (22); having a check unit (23) for checking the validity of the at least one data record (12) as recited in one of the preceding claims.

11. The processor unit as recited in Claim 10,
wherein the processor unit (20) has a read-only code word memory (25), code words (25a, 25b, 25c, 25d) being stored in the code word memory (25) and a counter (24) having an incrementable counter content which points to one of the code words (25a, 25b, 25c, 25d) being assigned to the code word memory (25), and the processor unit (20) being individualized in particular via an identification sequence (14).

12. The processor unit as recited in one of Claims 10 through 11,

wherein the processor unit (20) is a control unit of a motor vehicle.